What is claimed is:

1. A method for forming a semiconductor device, comprising steps of:

a) forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

b) forming a metal interconnection in the metal interconnection region of the insulation layer by performing a dual damascene process; and

c) forming a capacitor in the capacitor region of said insulation layer such that said capacitor is in a same level as the metal interconnection in the insulation layer.

2. The method as recited in claim 1, wherein the step c) includes steps of:

c-1) forming a first trench at the capacitor region of the insulation layer;

c-2) forming a first metal interconnection inside the first trench;

c-3) forming a second trench by removing the insulation layer between the first metal interconnection; and

c-4) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of said second trench.

3. The method as recited in claim 1, wherein the step c) includes steps of:

c-1) forming a first trench in the capacitor region of the insulation layer;

c-2) forming a first barrier metal and a first metal interconnection inside the first trench;

c-3) forming a second trench by removing the insulation layer around the first barrier metal;

c-4) forming a third trench in the first barrier metal by removing the first metal interconnection; and

c-5) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the second and the third trenches.

4. The method as recited in claim 2, further comprising the step of forming a second metal interconnection connected to the second electrode of the capacitor.

5. The method as recited in claim 2, wherein the first metal interconnection is made of copper.

6. The method as recited in claim 2, wherein the first and the second electrodes are made of a metal selected from the group consisting of Pt, Ru, Ir and W.

7. The method as recited in claim 2, wherein the dielectric layer is made of an oxide selected from the group consisting of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and combinations thereof.

8. A method for fabricating a semiconductor device, comprising steps of:

a) forming an insulation layer including a first insulation layer and a second insulation layer in a capacitor region and a metal interconnection region on a substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer;

c) forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing a resulting structure;

d) forming a second trench by selectively etching the second insulation layer in the capacitor region;

e) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the second trench; and

f) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing said second copper layer.

9. The method as recited in claim 8, wherein the step of forming the insulation layer includes forming an etching blocking layer between the first insulation layer and the

second insulation layer.

10. The method as recited in claim 8, further including forming a hard mask on the second insulation layer.

11. The method as recited in claim 8, wherein the step of b) forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer first forms the interconnection trench and the first trench simultaneously, and then forms the via hole.

12. The method as recited in claim 8, wherein the step of b) forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer first forms the via hole, and then forms the interconnection trench and the first trench simultaneously.

13. The method as recited in claim 8, wherein the first and the second copper layers are formed using a reflow method after forming a layer in a sputtering method, a CVD method or an electroplating method.

14. The method as recited in claim 13, wherein using the electroplating method, a seed layer is formed by a method selected from the group consisting of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

15. The method as recited in claim 8, further including the steps of:

g) forming a first barrier metal prior to the first copper layer; and

h) forming a second barrier metal prior to the second copper layer.

16. A method for fabricating a semiconductor device, comprising steps of:

a) forming an insulation layer including a first insulation layer and a second insulation layer in a metal interconnection region and a capacitor region on a substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench and planarizing a resulting structure;

d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region;

e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the second and third trenches; and

g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing said second copper layer.

17. The method as recited in claim 16, wherein a second barrier metal is formed prior to forming of the second copper layer.

18. The method as recited in claim 16, wherein the first and the second barrier metals are made of one selected from the group consisting of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and combinations thereof.

19. A semiconductor device, comprising:

a substrate;

an insulation layer formed in a metal interconnection region and a capacitor region on the substrate;

a metal interconnection in the insulation layer of the metal interconnection region; and

a capacitor formed in the capacitor region of the insulation layer in a same level as the metal interconnection.

20. The semiconductor device as recited in claim 19, wherein the capacitor includes:

a first metal interconnection;

a trench formed between parts of the first metal interconnection; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the trench.

21. The semiconductor device as recited in claim 19, wherein the capacitor includes:

a barrier metal with a first trench inside;

a second trench formed between portions of the barrier metal; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the first and second trenches.

22. The semiconductor device as recited in claim 20, further including a second metal interconnection connected to the second electrode of the capacitor.

23. The semiconductor device as recited in claim 22, wherein the first and the second metal interconnections are formed by depositing a copper layer and a barrier metal.

24. The semiconductor device as recited in claim 19, wherein the insulation layer is made of a material selected from the group consisting of SiO_2, SiOC, SiOH, SiOCH,

insulation layers with dielectric constants below 3.0, and combinations thereof.

25. The semiconductor device as recited in claim 20, wherein the dielectric layer is made of an oxide selected from the group consisting of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and combinations thereof.

26. The semiconductor device as recited in claim 20, wherein the first and the second electrodes are made of a metal selected from the group consisting of Pt, Ru, Ir and W.

27. The semiconductor device as recited in claim 23, wherein the barrier metal is made of a material selected from the group consisting of Ta, TaN, TiN, WN, TaC, WC, TiSiN, TaSiN, and combinations thereof.